INTEGRATED CIRCUITS

DATA SHEET

TDA8559
Low-voltage stereo headphone amplifier

Preliminary specification
File under Integrated Circuits, IC01

1996 Jan 02

Philips Semiconductors

PHILIPS

Low-voltage stereo headphone amplifier TDA8559

FEATURES

- Operating voltage from 1.8 to 30 V
- Very low quiescent current
- Low distortion
- Few external components
- Differential inputs
- Usable as a mono amplifier in bridge-tied load (BTL) or stereo single-ended (SE)
- Single-ended mode without loudspeaker capacitor
- Mute and standby mode
- Short-circuit proof to ground, to supply voltage (<18 V) and across load
- No switch on or switch off clicks
- ESD protected on all pins.

APPLICATIONS

- Portable telephones
- Walk-man's
- Portable audio
- Mains fed equipment.

GENERAL DESCRIPTION

The TDA8559 is a stereo amplifier that operates over a wide supply voltage range from 1.8 to 30 V and consumes a very low quiescent current. This makes it suitable for battery fed applications (2 × 1.5 V cells). Because of an internal voltage buffer, this device can be used with or without a capacitor connected in series with the load. It can be applied as a headphone amplifier, but also as a mono amplifier with a small speaker (25 W), or as a line driver in mains applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	operating supply voltage		1.8	3	30	V
$I_{q(tot)}$	total quiescent current		–	2.75	4	mA
I_{stb}	standby supply current		–	–	10	μA
Stereo application						
P_o	output power	THD = 10%	30	35	–	mW
THD	total harmonic distortion	P_o = 20 mW; f_i = 1 kHz	–	0.05	0.1	%
		P_o = 20 mW; f_i = 10 kHz	–	0.1	–	%
G_v	voltage gain		25	26	27	dB
f_{ss}	small signal roll-off frequency	–1 dB	–	750	–	kHz
BTL application						
P_o	output power	THD = 10%	125	140	–	mW
THD	total harmonic distortion	P_o = 20 mW; f_i = 1 kHz	–	0.075	0.15	%
		P_o = 20 mW; f_i = 10 kHz	–	0.2	–	%
G_v	voltage gain		31	32	33	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8559	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TDA8559T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

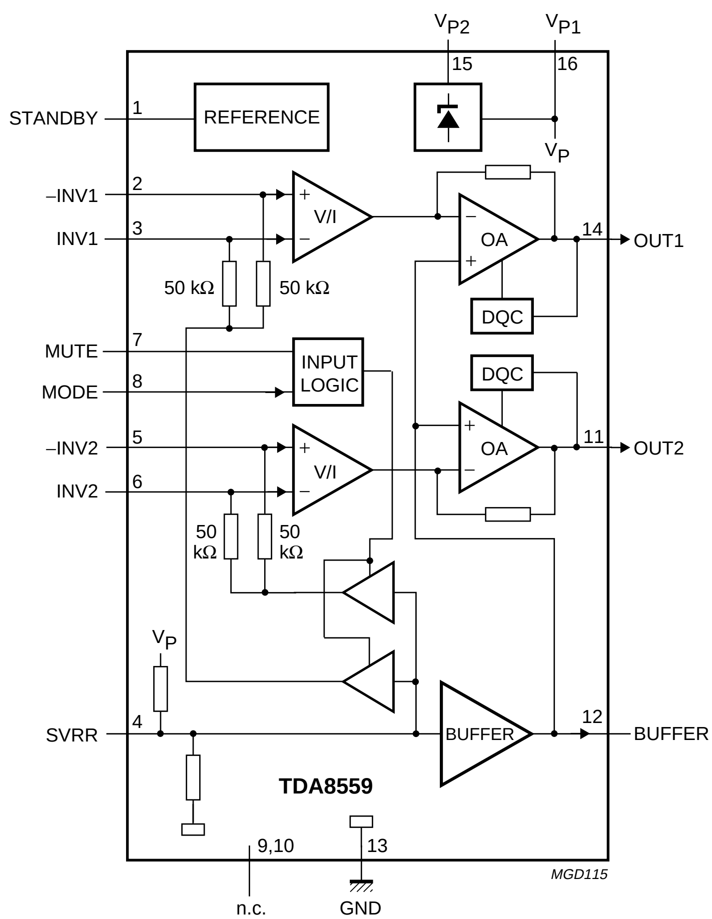


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
STANDBY	1	standby select
–INV1	2	non-inverting input 1
INV1	3	inverting input 1
SVRR	4	supply voltage ripple rejection
–INV2	5	non-inverting input 2
INV2	6	inverting input 2
MUTE	7	mute select
MODE	8	input mode select
n.c.	9	not connected
n.c.	10	not connected
OUT2	11	output 2
BUFFER	12	buffer output ($0.5V_P$)
GND	13	ground
OUT1	14	output 1
V_{P2}	15	high supply voltage
V_{P1}	16	low supply voltage

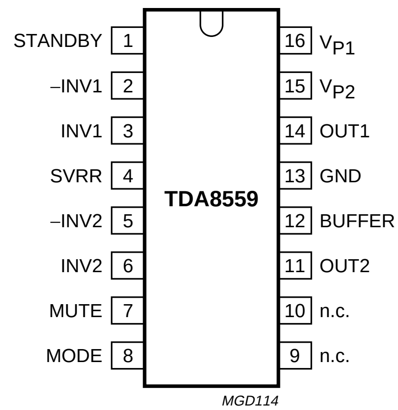


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8559 contains two amplifiers with differential inputs, a $0.5V_P$ output buffer and a high supply voltage stabiliser. Each amplifier consist of a voltage-to-current converter (V/I), an output amplifier and its dynamic quiescent controller. The gain of each amplifier is internally fixed at 26 dB (= 20 ×). The $0.5V_P$ output can be used as a replacement for the single-ended capacitors. The two amplifiers can also be used as a mono amplifier in a bridge-tied load (BTL) configuration thereby resulting in more output power.

With three mode select pins, the device can be switched into the following modes;

1. Standby mode (I_P < 10 µA)
2. Mute mode
3. Operation mode, with two input selections (the input source is directly connected or connected via a coupling capacitor at the input).

The ripple rejection in the stereo application with a single-ended capacitor can be improved by connecting a capacitor between the $0.5V_P$ capacitor pin and ground.

The device is fully protected against short-circuiting of the output pins to ground, to the low supply voltage pin and across the load.

V/I converters

The V/I converters have a transconduction of 400 µS. The inputs are completely symmetrical and the two amplifiers can be used in opposite phase. The mute mode causes the V/I converters to block the input signal. The input mode pin selects two applications in which the V/I converters can be used.

The first application (input mode pin floating) is used with a supply voltage below 6 V. The input DC level is at ground level (the unused input pin connected to ground) and no input coupling capacitors are necessary. The maximum converter output current is sufficient to obtain an output swing of 3 V (peak).

In the second application with a supply voltage greater than 6 V (input mode pin high), the input mode pin is connected to V_P. In this configuration (input DC level = $0.5V_P$ + 0.6 V) the input source must be coupled with a capacitor and the two unused input pins must be connected via a capacitor to ground, to improve noise performance. This application has a higher quiescent current, because the maximum output current of the V/I converter is higher to obtain an output voltage swing of 9 V (peak).

Output amplifiers

The output amplifiers have a transresistance of 50 kΩ, a bandwidth of approximately 750 kHz and a maximum output current of 150 mA. The mid-tap output voltage equals the voltage applied at the non-inverting pin of the output amplifier. This pin is connected to the output of the $0.5V_P$ buffer. This reduces the distortion when the load is connected between an output amplifier and the buffer (because feedback is applied over the load).

Buffer

The buffer delivers $0.5V_P$ to the output with a maximum output (sink and source) current of 300 mA (peak).

Dynamic quiescent controller

The Dynamic Quiescent Current controller (DQC) gives the advantage of low quiescent current and low distortion. When there are high frequencies in the output signal, the DQC will increase the quiescent current of its own output amplifier. This will reduce the cross-over distortion that normally occurs at high frequencies and low quiescent current. The DQC gives two output currents that are linear with the amplitude and the frequency of the output signal of its own output amplifier. These currents control the quiescent current.

Stabilizer

The TDA8559 has a voltage supply range from 1.8 to 30 V. This range is divided over two supply voltage pins. Pin 16 is 1.8 to 18 V (breakdown voltage of the process); this pin is preferred for supply voltages less than 18 V. Pin 15 is used for applications where V_P is approximately 6 to 30 V. The stabilizer output is internally connected to the supply voltage pin 16 and in the range from 6 to 18 V to pin 15. The voltage drop to pin 16 is 1 V. In the range from 18 to 30 V the stabilizer output voltage (to pin 16) is approximately 17 V.

Input logic

The mute pin (pin 7) selects the mute mode of the V/I converters. Low (TTL/CMOS) level is mute. A voltage between 0.5 V (low level) and 1.5 V (high level) causes a soft mute to operate (no plops). When pin 7 is floating or greater than 1.5 V it is in the operating condition.

The input mode pin must be connected to V_P when the supply voltage is greater than 6 V. The input mode logic raises the tail current of the V/I converters and enables the two buffers to bias the inputs of the V/I converters.

Reference

This circuit supplies all currents needed in this device. With the standby mode pin 1 (TTL/CMOS), it is possible to switch to the standby mode and reduce the total quiescent current to below 10 μA.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{P2(max)}$	maximum supply voltage (pin 15)		–	30	V
$V_{P1(max)}$	maximum supply voltage (pin 16)		–	18	V
$V_{i(max)}$	maximum input voltage		–	18	V
I_{ORM}	peak output current	repetitive	–	150	mA
P_{tot}	total power dissipation	SO16	–	1.19	W
		DIP16	–	2.4	W
T_{amb}	operating ambient temperature		–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	150	°C
t_{sc}	short-circuiting time		–	1	hour

QUALITY SPECIFICATION

Quality in accordance with *“UZW-FQ-611*”, if this type is used as an audio amplifier. The number of the quality specification can be found in the *“Quality Reference handbook”*. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

SYMBOL	DESCRIPTION	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	DIP16	52	K/W
	SO16	105	K/W

CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C; f_i = 1 kHz; unless otherwise specified).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC characteristics						
V_P	operating supply voltage	note 1	1.8	3	30	V
$I_{q(tot)}$	total quiescent current	open load	–	2.75	4	mA
I_{stb}	standby supply current	open load	–	–	10	µA
V_1	standby mode voltage	standby	0	–	0.5	V
		operating	1.5	–	18	V
V_7	mute mode voltage	mute	0	–	0.5	V
		operating	1.5	–	18	V
I_{bias}	input bias current		–	100	300	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Single-ended stereo application (R_L = 32 Ω)						
P_o	output power	THD = 10%	30	35	–	mW
THD	total harmonic distortion	P_o = 20 mW; f_i = 1 kHz; note 2	–	0.05	0.1	%
		P_o = 20 mW; f_i = 10 kHz; note 2	–	0.1	–	%
G_v	voltage gain		25	26	27	dB
f_{ss}	small signal roll-off frequency	–1 dB	–	750	–	kHz
α_{cs}	channel separation	R_s = 5 kΩ	40	–	–	dB
$\lvert\Delta G_v\rvert$	channel unbalance		–	–	1	dB
V_{no}	noise output voltage	note 3	–	75	90	μV
$V_{no(mute)}$	noise output voltage in mute	note 3	–	35	45	μV
$V_{o(mute)}$	output voltage in mute	note 4	–	–	45	μV
V_{mt}	mid-tap voltage		1.4	1.5	1.6	V
Z_i	input impedance		75	100	125	kΩ
V_{os}	DC output offset voltage	note 5	–	–	100	mV
SVRR	supply voltage ripple rejection	note 6	45	–	–	dB
BTL application (R_L = 25 Ω)						
P_o	output power	THD = 10%	125	140	–	mW
THD	total harmonic distortion	P_o = 20 mW; f_i = 1 kHz; note 2	–	0.075	0.15	%
		P_o = 20 mW; f_i = 10 kHz; note 2	–	0.2	–	%
G_v	voltage gain		31	32	33	dB
f_{ss}	small signal roll-off frequency	–1 dB	–	750	–	kHz
V_{no}	noise output voltage	note 3	–	100	120	μV
$V_{no(mute)}$	noise output voltage in mute	note 3	–	50	60	μV
$V_{o(mute)}$	output voltage in mute	note 4	–	–	60	μV
V_{os}	DC output offset voltage	note 7	–	–	150	mv
SVRR	supply voltage ripple rejection	note 6	44	–	–	dB
Z_i	input impedance		39	50	61	kΩ
Line driver application (R_L = 1 kΩ)						
V_o	line output voltage		0.1	–	2.9	V

Note

1. The supply voltage range at pin V_{P1} is from 1.8 to 18 V. Pin V_{P2} is used for the voltage range from 6 to 30 V.
2. Measured with low-pass filter 30 kHz.
3. Noise output voltage measured with a bandwidth of 20 Hz to 20 kHz, unweighted. R_s = 5 kΩ
4. RMS output voltage in mute is measured with V_i = 200 mV (RMS); f = 1 kHz.
5. DC output offset voltage is measured between the signal output and the $0.5V_P$ output.
6. The ripple rejection is measured with a ripple voltage of 200 mV (RMS) applied to the positive supply rail (R_s = 0 kΩ).
7. DC output offset voltage is measured between the two signal outputs.

TEST AND APPLICATION INFORMATION

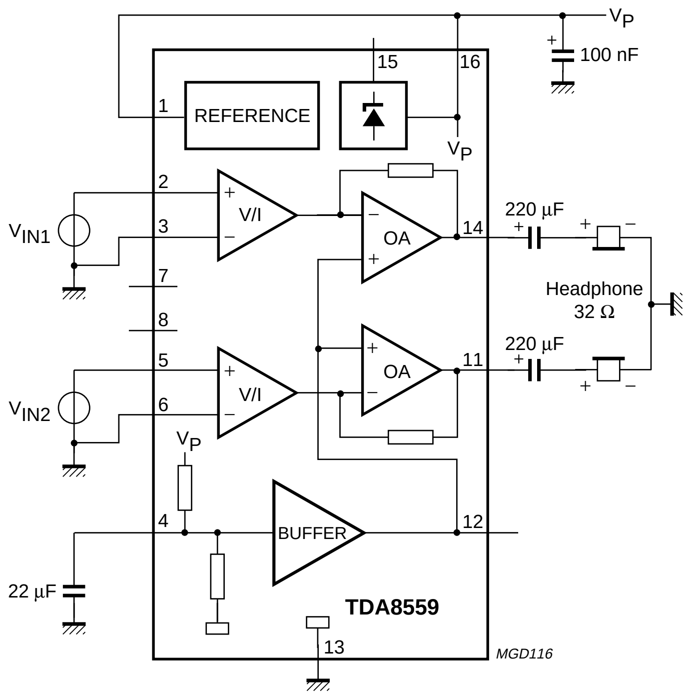


Fig.3 Single-ended with loudspeaker capacitor.

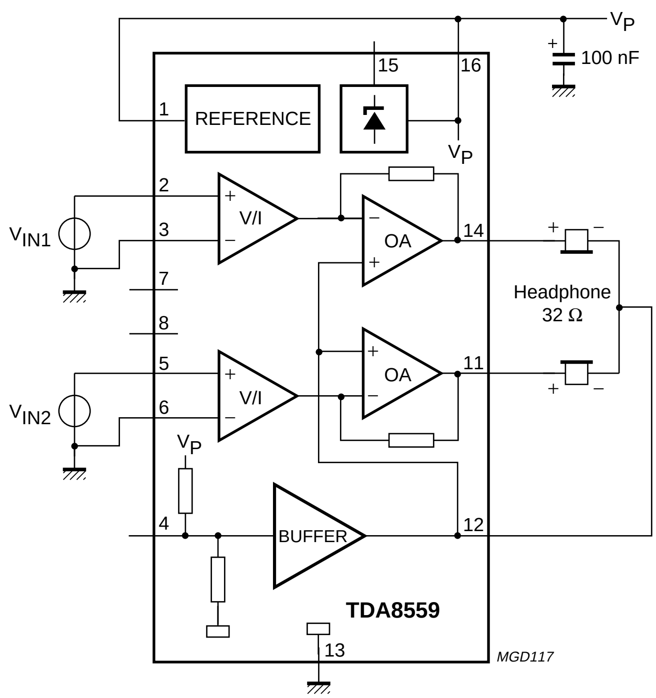


Fig.4 Single-ended with buffer.

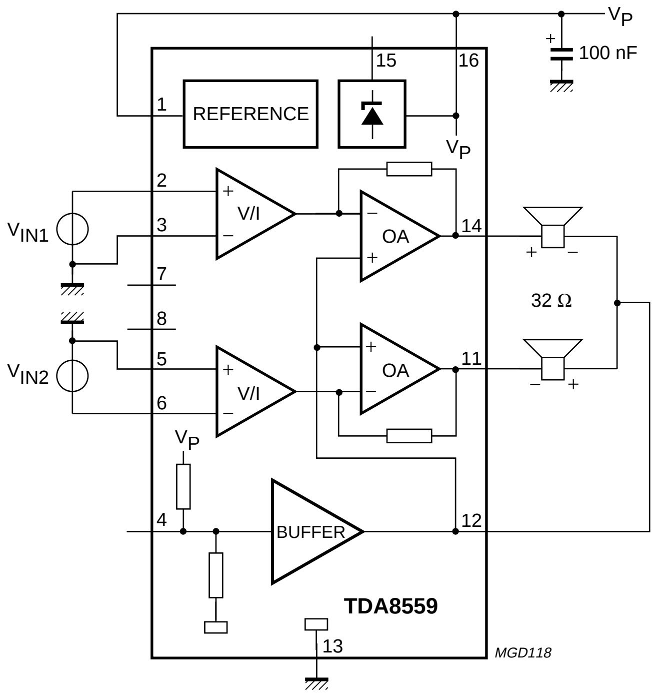


Fig.5 Improved single-ended with buffer.

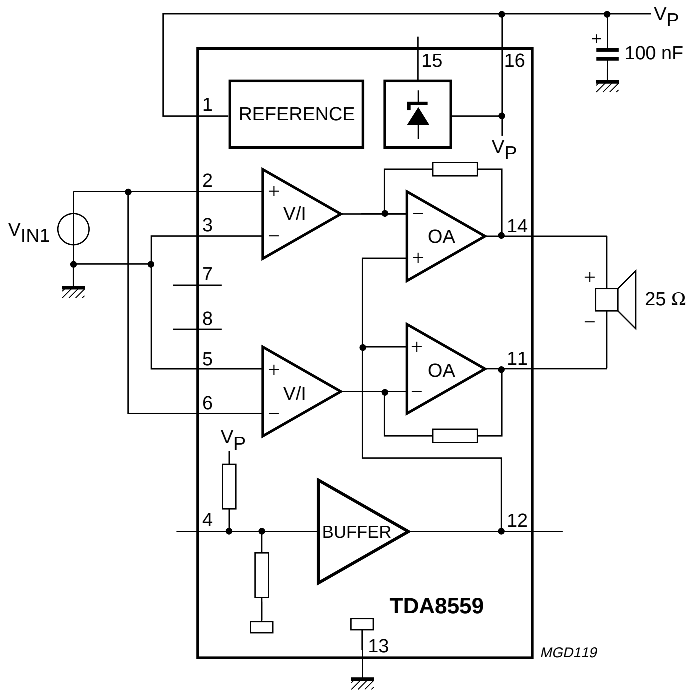


Fig.6 BTL amplifier.

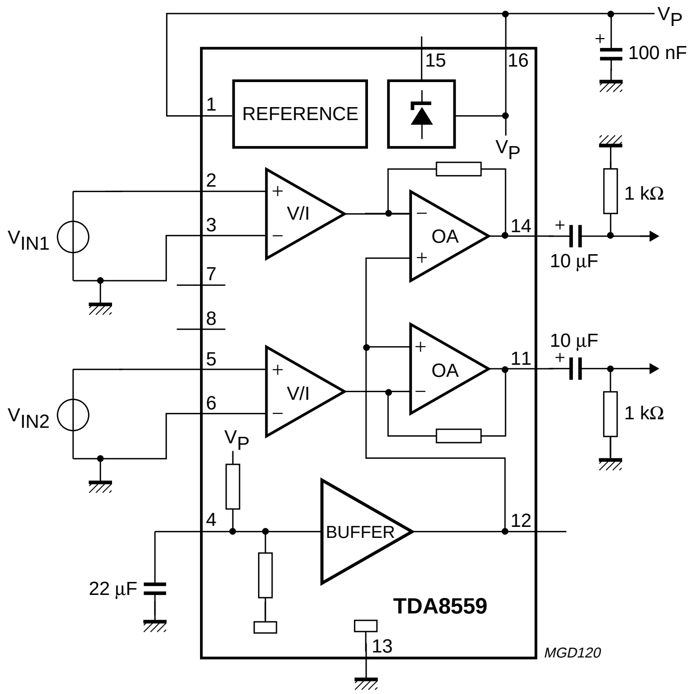


Fig.7 Line driver application 1.8 to 6 V.

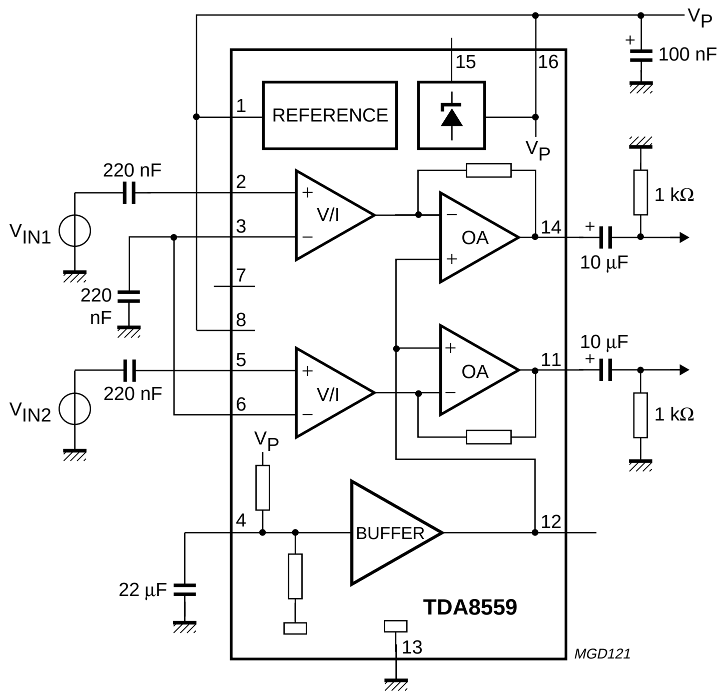


Fig.8 Line driver application V_P = 6 to 18 V.

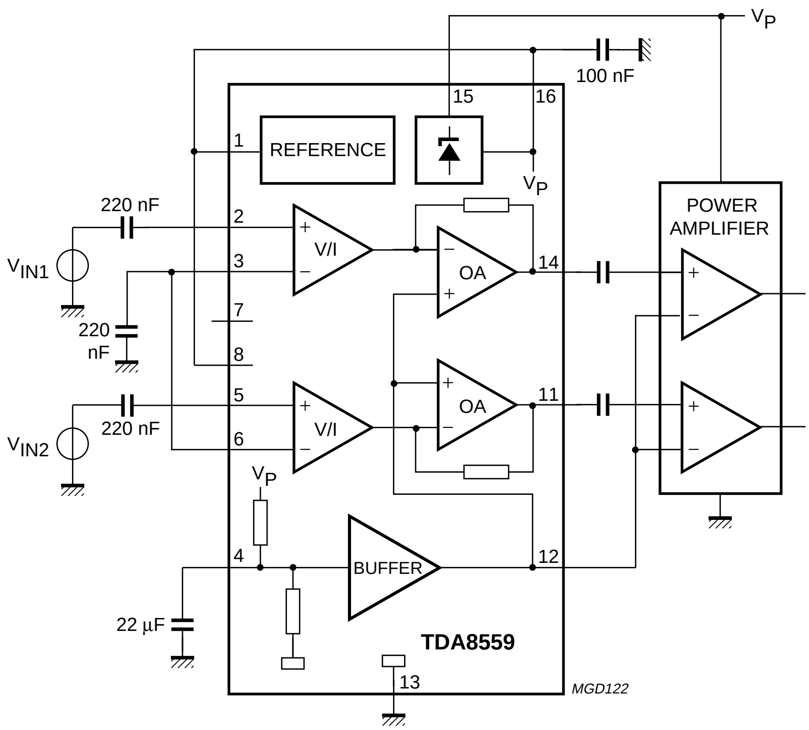


Fig.9 Line driver application V_P = 6 to 30 V.

Application notes

GENERAL

For applications where V_P has a maximum voltage of 6 V (input mode low), the input pins need a DC path to ground, see Fig.10 and Fig.11 for applications where V_P has a voltage range of 6 to 18 V (input mode high) the input DC level is $0.5V_P$ + 0.6 V, see Fig.12 and Fig.13.

APPLICATION 1 (see Fig.3)

This is the basic headphone application with four external components. In this configuration the headphone amplifier can deliver a peak output current of 100 mA.

APPLICATION 2 (see Fig.4)

The advantage of this application, with respect to Application 1, is that it has only one external component and maintains the same performance.

APPLICATION 3 (see Fig.5)

This application is an improved version of application 2. The difference is connecting the two loads in opposite phase. This lowers the average current through the single-ended buffer. A headphone cannot be used because it is necessary that the load has floating terminals.

APPLICATION 4 (see Fig.6)

This configuration delivers four times the output power of the single-ended application with the same load conditions. The disadvantage is that the load must have floating terminals consequently a stereo headphone application is not possible.

APPLICATION 5 (see Fig.7)

The TDA8559 has a virtual rail-to-rail output voltage and is also usable in a low voltage environment such as a line driver. In this application the input needs a DC path to ground; input configurations illustrated in Fig.10 or Fig.11 have to be used.

APPLICATION 6 (see Fig.8)

The TDA8559 has a virtual rail-to-rail output voltage. Because the input mode is high, input configurations illustrated in Fig.12 or Fig.13 have to be used.

APPLICATION 7 (see Fig.9)

Using pin V_{P2} it is possible to use the headphone amplifier above the maximum 18 V supply voltage of pin V_{P1}. The internal supply voltage will be reduced to approximately 17 V. This is convenient in applications where there is a higher supply voltage than 18 V but do not need an output voltage swing that reaches the higher supply voltage; input configurations illustrated in Fig.12 or Fig.13 have to be used.

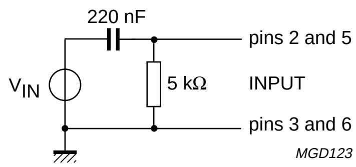


Fig.10 Input configuration; with input capacitor and $V_P < 6$ V.

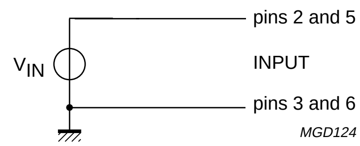


Fig.11 Input configuration; without input capacitor and $V_P < 6$ V.

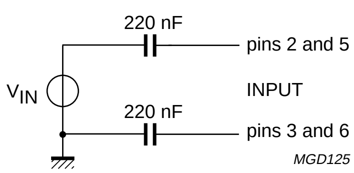


Fig.12 Input configuration; at $V_P > 6$ V.

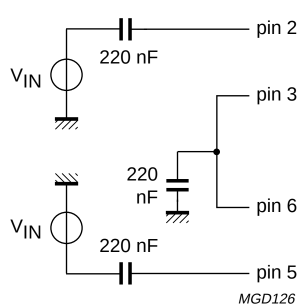
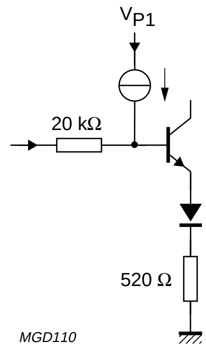
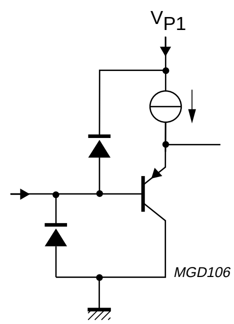
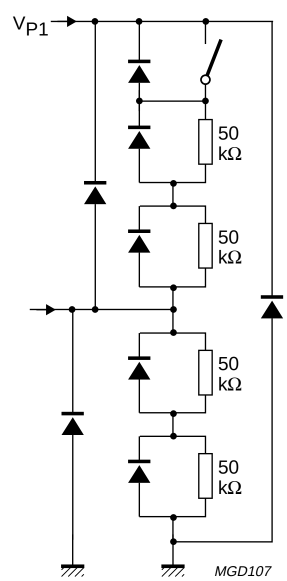
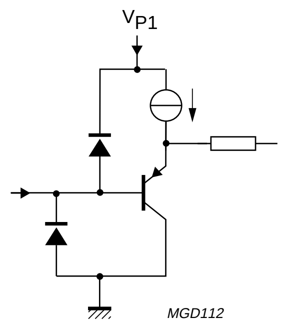
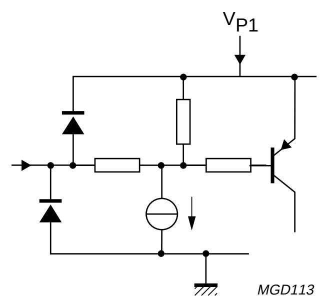
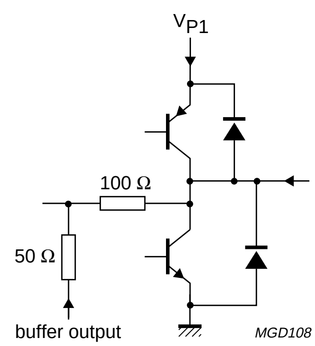
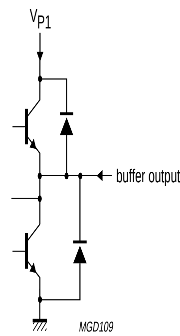
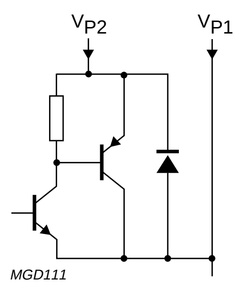


Fig.13 Input configuration; at $V_P > 6$ V (combined negative inputs).

INTERNAL PIN CONFIGURATION

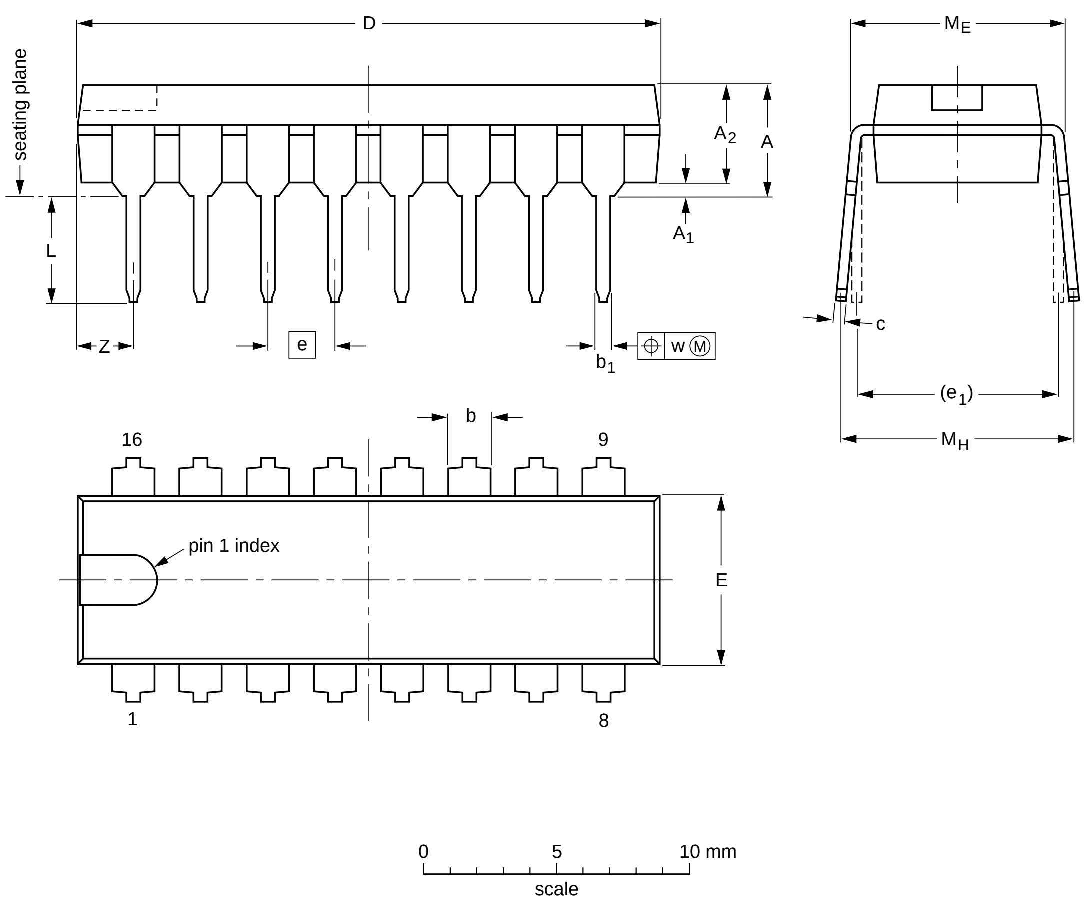
SYMBOL	PIN	EQUIVALENT CIRCUIT
STANDBY	1	
–INV1, INV1, –INV2 and INV2	2, 3, 5 and 6	
SVRR	4	

SYMBOL	PIN	EQUIVALENT CIRCUIT
MUTE	7	
MODE	8	
OUT2 and OUT1	11 and 14	

SYMBOL	PIN	EQUIVALENT CIRCUIT
BUFFER	12	
V_{P2} and V_{P1}	15 and 16	

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

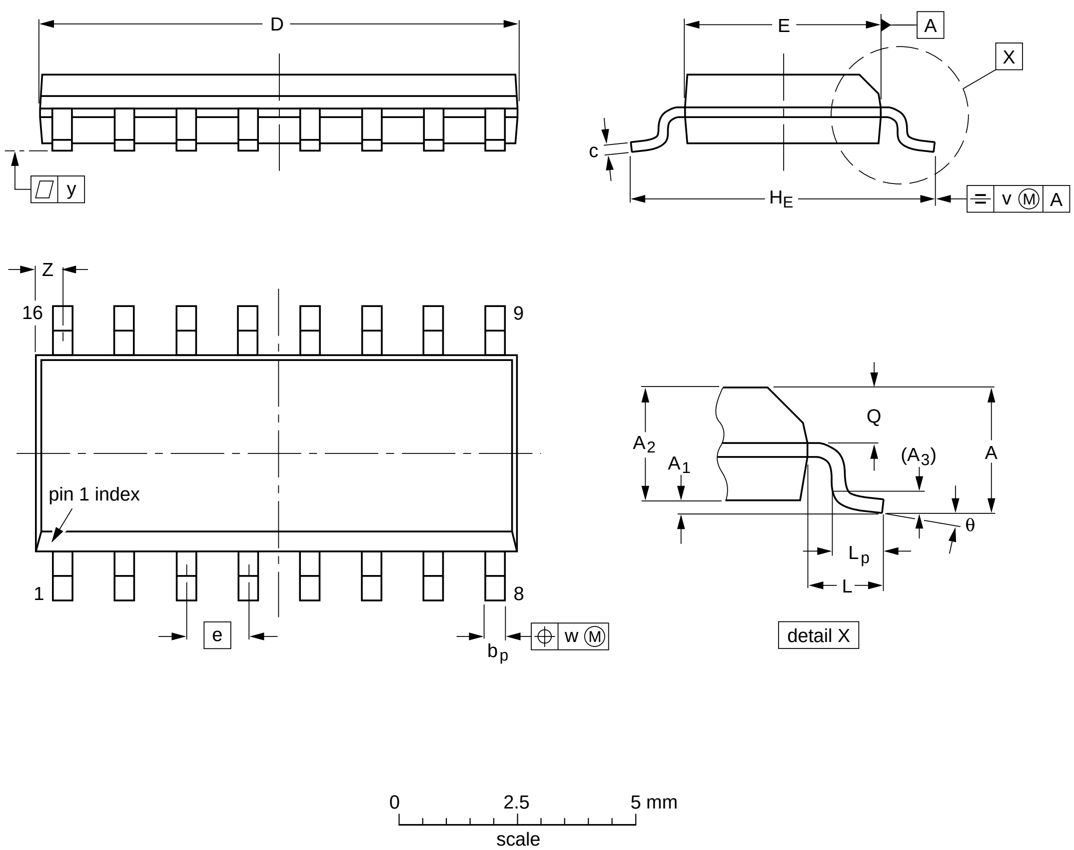
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**

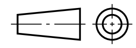


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Philips Semiconductors – a worldwide company

Argentina: IEROD, Av. Juramento 1992 - 14.b, (1428)
BUENOS AIRES, Tel. (541)786 7633, Fax. (541)786 9367

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. (02)805 4455, Fax. (02)805 4466

Austria: Triester Str. 64, A-1101 WIEN, P.O. Box 213,
Tel. (01)60 101-1236, Fax. (01)60 101-1211

Belgium: Postbus 90050, 5600 PB EINDHOVEN, The Netherlands,
Tel. (31)40-2783749, Fax. (31)40-2788399

Brazil: Rua do Rocio 220 - 5th floor, Suite 51,
CEP: 04552-903-SÃO PAULO-SP, Brazil,
P.O. Box 7383 (01064-970),
Tel. (011)821-2333, Fax. (011)829-1849

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS:
Tel. (800) 234-7381, Fax. (708) 296-8556

Chile: Av. Santa Maria 0760, SANTIAGO,
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China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. (852)2319 7888, Fax. (852)2319 7700

Colombia: IPRELENSO LTDA, Carrera 21 No. 56-17,
77621 BOGOTA, Tel. (571)249 7624/(571)217 4609,
Fax. (571)217 4549

Denmark: Prags Boulevard 80, PB 1919, DK-2300
COPENHAGEN S, Tel. (45)32 88 26 36, Fax. (45)31 57 19 49

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. (358)0-615 800, Fax. (358)0-61580 920

France: 4 Rue du Port-aux-Vins, BP317,
92156 SURESNES Cedex,
Tel. (01)4099 6161, Fax. (01)4099 6427

Germany: P.O. Box 10 51 40, 20035 HAMBURG,
Tel. (040)23 53 60, Fax. (040)23 53 63 00

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. (01)4894 339/4894 911, Fax. (01)4814 240

India: Philips INDIA Ltd, Shivsagar Estate, A Block,
Dr. Annie Besant Rd. Worli, Bombay 400 018
Tel. (022)4938 541, Fax. (022)4938 722

Indonesia: Philips House, Jalan H.R. Rasuna Said Kav. 3-4,
P.O. Box 4252, JAKARTA 12950,
Tel. (021)5201 122, Fax. (021)5205 189

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. (01)7640 000, Fax. (01)7640 200

Italy: PHILIPS SEMICONDUCTORS S.r.l.,
Piazza IV Novembre 3, 20124 MILANO,
Tel. (0039)2 6752 2531, Fax. (0039)2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. (03)3740 5130, Fax. (03)3740 5077

Korea: Philips House, 260-199 Itaewon-dong,
Yongsan-ku, SEOUL, Tel. (02)709-1412, Fax. (02)709-1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA,
SELANGOR, Tel. (03)750 5214, Fax. (03)757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TX 79905,
Tel. 9-5(800)234-7381, Fax. (708)296-8556

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. (040)2783749, Fax. (040)2788399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. (09)849-4160, Fax. (09)849-7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. (022)74 8000, Fax. (022)74 8341

Pakistan: Philips Electrical Industries of Pakistan Ltd.,
Exchange Bldg. ST-2/A, Block 9, KDA Scheme 5, Clifton,
KARACHI 75600, Tel. (021)587 4641-49,
Fax. (021)577035/5874546

Philippines: PHILIPS SEMICONDUCTORS PHILIPPINES Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. (63) 2 816 6380, Fax. (63) 2 817 3474

Portugal: PHILIPS PORTUGUESA, S.A.,
Rua dr. António Loureiro Borges 5, Arquiparque - Miraflores,
Apartado 300, 2795 LINDA-A-VELHA,
Tel. (01)4163160/4163333, Fax. (01)4163174/4163366

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. (65)350 2000, Fax. (65)251 6500

South Africa: S.A. PHILIPS Pty Ltd.,
195-215 Main Road Martindale, 2092 JOHANNESBURG,
P.O. Box 7430, Johannesburg 2000,
Tel. (011)470-5911, Fax. (011)470-5494

Spain: Balmes 22, 08007 BARCELONA,
Tel. (03)301 6312, Fax. (03)301 42 43

Sweden: Kottbygatan 7, Akalla. S-164 85 STOCKHOLM,
Tel. (0)8-632 2000, Fax. (0)8-632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. (01)488 2211, Fax. (01)481 77 30

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66, Chung Hsiao West
Road, Sec. 1. Taipeh, Taiwan ROC, P.O. Box 22978,
TAIPEI 100, Tel. (886) 2 382 4443, Fax. (886) 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong,
Bangkok 10260, THAILAND,
Tel. (66) 2 745-4090, Fax. (66) 2 398-0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. (0212)279 27 70, Fax. (0212)282 67 07

Ukraine: Philips UKRAINE, 2A Akademika Koroleva str., Office 165,
252148 KIEV, Tel. 380-44-4760297, Fax. 380-44-4766991

United Kingdom: Philips Semiconductors LTD.,
276 Bath Road, Hayes, MIDDLESEX UB3 5BX,
Tel. (0181)730-5000, Fax. (0181)754-8421

United States: 811 East Arques Avenue, SUNNYVALE,
CA 94088-3409, Tel. (800)234-7381, Fax. (708)296-8556

Uruguay: Coronel Mora 433, MONTEVIDEO,
Tel. (02)70-4044, Fax. (02)92 0601

Internet: http://www.semiconductors.philips.com/ps/

For all other countries apply to: Philips Semiconductors,
International Marketing and Sales, Building BE-p,
P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands,
Telex 35000 phtcnl, Fax. +31-40-2724825

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